WHAT IS CLAIMED IS:

1. A device for recording the block status information of a nonvolatile memory, comprising:

an interface unit electrically connected to at least one nonvolatile memory including a plurality of blocks, each being a basic unit for erasing data of said at least one nonvolatile memory;

a processor connected to said interface unit through which the status of a block of said at least one nonvolatile memory is detected to obtain the block status information; and

a memory unit connected to said processor for temporarily storing said block status information which is then written into one of said plurality of blocks by means of said processor through said interface unit after the end of the detection.

2. The device for recording the block status information of claim 1, further comprising a counter for counting the number of the blocks of said at least one nonvolatile memory when said processor detects the status of the blocks of said at least one nonvolatile memory to obtain a counter value so that said processor writes said counter value into said at least one nonvolatile memory after the end of the detection.

3. The device for recording the block status information of claim 2, wherein said counter value is the number of valid blocks or invalid blocks.

4. The device for recording the block status information of claim 1, wherein said recorded block status information includes at least one valid block address.

5. The device for recording the block status information of claim 1, wherein said recorded block status information includes at least one invalid block address.

6. The device for recording the block status information of claim 1, wherein said interface unit is a host device.

7. The device for recording the block status information of claim 5, wherein said host device is an integrated circuit (IC) socket.

8. The device for recording the block status information of claim 1, wherein one of said plurality of blocks is the first block (Block 0).

9. The device for recording the block status information of claim 1, wherein said processor provides at least one error correction code (ECC) and records said at least one ECC together with said block status information to ensure the correct access of the block status information.

10. The device for recording the block status information of claim 1, wherein said memory unit is a random access memory (RAM).

11. The device for recording the block status information of claim 1, wherein said at least one nonvolatile memory is a NAND-type flash memory.

12. A method for recording the block status information of a nonvolatile memory, comprising the following steps:

(A) performing an initialization to set at least one reference value;

(B) detecting at least one nonvolatile memory having a plurality of blocks to obtain the status of at least one block which is a basic unit for

erasing data of the at least one nonvolatile memory; and

(C) writing the detected information into a memory unit until the end of the detection, and then writing said at least one block status information into one of the blocks of said at least one nonvolatile memory.

13. The method of claim 12, wherein a counter for counting the number of the detected blocks is further used at step (B) to obtain a counter value to be written into said at least one nonvolatile memory after the end of the detection.

14. The method of claim 12, wherein said at least one reference value comprises the initial address of said nonvolatile memory, the counter value of said counter and the initial address of said memory unit.

15. The method of claim 12, wherein said at least one detected information is at least one valid block address.

16. The method of claim 12, wherein said at least one detected information is at least one invalid block address.

17. The method of claim 12, wherein one of the blocks is the first block (Block 0).

18. The method of claim 12, wherein writing of at least one error correction code (ECC) together with block status information to ensure the correct access of the block status information.

19. The method of claim 12, wherein said at least one nonvolatile memory is a NAND-type flash memory.

20. The method of claim 19, wherein said flash memory is a NAND-type flash memory.

21. The method of claim 12, wherein said memory unit is a random access memory (RAM).